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METHOD AND APPARATUS FOR ROUTING DIFFERENTIAL SIGNALS ACROSS A SEMICONDUCTOR CHIP

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[0001] This invention was made with United States Government support under Contract No. NBCH020055 awarded by the Defense Advanced Research Projects Administration. The United States Government has certain rights in the invention.

BACKGROUND

Field of the Invention

[0002] The present invention relates to techniques for routing signals across a semiconductor chip. More specifically, the present invention relates to a method and an apparatus for routing differential signals across a semiconductor chip in a manner that reduces effective capacitance and differential coupling.

Related Art

[0003] As processor clock speeds continue to increase at an exponential rate, data must be transferred at correspondingly faster rates between computer system components. This can be a problem for conventional bus structures because the faster switching speeds and smaller voltage swings in the latest generation of semiconductor chips cause signal lines to be more sensitive to noise.

[0004] To remedy this problem, designers are beginning to use differential signaling to transmit signals across a semiconductor chip. Differential signaling uses two signal lines to carry a "true" and "complement" version of each signal, wherein the value of the signal is indicated by the voltage difference between the two signal lines. Because currents are balanced between power and ground rails, differential signaling reduces power supply noise and effectively provides return currents. Moreover, differential signaling is less sensitive to ground shifts (or other common mode noise) between sender and receiver because differential signaling relies on voltage differences between pairs of signal lines, instead of relying on an absolute voltage level of a single signal line.

[0005] As the demand for higher bandwidth continues to increase, designers are beginning to pack differential wires tightly together to increase the total number of communication channels. However, when differential wires are packed tightly together, they can potentially interfere with each other through energy coupling, which can have deleterious effects on performance and reliability. For example, FIG. 1 illustrates a differential pair of wires, A and $\overline{A}$, which carry complementary signals. Hence, if A moves up, $\overline{A}$ moves down, and vice versa. The differential pair, B and $\overline{B}$, operates in the same manner. Note that these differential pairs typically belong to a wider signal bus, which includes additional differential pairs of the same length that run in the same direction.

[0006] In the arrangement of wires as illustrated in FIG. 1, signals in neighboring wires can potentially interfere with each other. For example, if a signal in wire B moves up, the corresponding complement signal in wire $\overline{B}$ moves down. Since wire $\overline{A}$ is adjacent to wire B, this can couple energy into wire $\overline{A}$, which can potentially cause errors or reduce performance. Furthermore, note that signals in wires $\overline{A}$ and B can disturb each along the entire length of the wires.

[0007] In order to remedy this problem, designers sometimes "twist" differential pairs of wires. For example, FIG. 2 illustrates a "fully-twisted" wiring scheme. In this fully-twisted scheme, if wire B moves up, it couples wire $\overline{A}$ upwards for ¼ of the wire length, but it also couples wire A upwards for ¼ of the wire length. At the same time, wire $\overline{A}$ has the same downward effect on both B and $\overline{B}$. Hence, the net coupling effect is zero in the first order.

[0008] Note, however, that wires A and $\overline{A}$ (and wires B and $\overline{B}$) are adjacent, and typically with minimal spacing. The line-to-line capacitance of two adjacent wires in a modern technology is approximately 70% of the total capacitance of the wire. In addition, the effective capacitance between any two physical structures doubles when the voltage on those two structures swings in opposite directions. Consequently, this fully-twisted scheme doubles the wire-to-wire "effective" capacitance seen by each wire, thereby causing higher power dissipation as well as longer delay.

[0009] Hence, what is needed is a method and an apparatus for routing differential signals across a semiconductor chip in a manner that reduces effective capacitance as well as differential coupling.

SUMMARY

[0010] One embodiment of the present invention provides an arrangement of differential pairs of wires that carry differential signals across a semiconductor chip. In this arrangement, differential pairs of wires are organized within a set of parallel tracks on the semiconductor chip. Furthermore, differential pairs of wires are organized to be non-adjacent within the tracks. This means that each true wire is separated from its corresponding complement wire by at least one intervening wire in the set of parallel tracks, thereby reducing coupling capacitance between corresponding true and complement wires. Moreover, this arrangement may include one or more twisting structures, wherein a twisting structure twists a differential pair of wires so that the corresponding true and complement wires are interchanged within the set of parallel tracks.

[0011] In a variation on this embodiment, the one or more twisting structures are arranged so that substantially zero net differential coupling capacitance exists for each differential pair of wires.

[0012] In a variation on this embodiment, the set of parallel tracks includes a possibly repeating pattern of four adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track. Furthermore, the differential pairs of wires include a first differential pair, A and $\overline{A}$, and a second differential pair, B and $\overline{B}$, wherein A starts in the first track, B starts in the second track, $\overline{A}$ starts in the third track and $\overline{B}$ starts in the fourth track. A first twisting structure causes B and $\overline{B}$ to interchange, so that A is in the first track, $\overline{B}$ is in the second track, $\overline{A}$ is in the third track and B is in the fourth track. A second twisting structure causes A and $\overline{A}$ to interchange, so that $\overline{A}$ is in the first track, $\overline{B}$ is in the second track, A is in the third track and B is in the fourth track. Finally, a third twisting structure

causes $\overline{B}$ and B to interchange, so that $\overline{A}$ is in the first track, B is in the second track, A is in the third track and $\overline{B}$ is in the fourth track.

[0013] In a variation on this embodiment, the first twisting structure is located approximately one quarter of the way down the set of parallel tracks; the second twisting structure is located approximately one half of the way down the set of parallel tracks; and the third twisting structure is located approximately three quarters of the way down the set of parallel tracks.

[0014] In a variation on this embodiment, the first twisting structure is located more than one quarter of the way down the set of parallel tracks; the second twisting structure is located more than one half of the way down the set of parallel tracks; and the third twisting structure is located more than three quarters of the way down the set of parallel tracks.

[0015] In a variation on this embodiment, the set of parallel tracks includes a possibly repeating pattern of four adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track. Furthermore, the differential pairs of wires include a first differential pair, A and $\overline{A}$, and a second differential pair, B and $\overline{B}$, wherein A starts in the first track, B starts in the second track, $\overline{A}$ starts in the third track and $\overline{B}$ starts in the fourth track. A first twisting structure causes A and $\overline{A}$ to interchange, so that $\overline{A}$ is in the first track, B is in the second track, A is in the third track and $\overline{B}$ is in the fourth track.

[0016] In a variation on this embodiment, the first twisting structure is located approximately one half of the way down the set of parallel tracks.

[0017] In a variation on this embodiment, the first twisting structure is located more than one half of the way down the set of parallel tracks.

[0018] In a variation on this embodiment, the set of parallel tracks includes a possibly repeating pattern of six adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track, which is adjacent to a fifth track, which is adjacent to a sixth track. Furthermore, the differential pairs of wires include a first differential pair, A and $\overline{A}$, a second differential pair, B and $\overline{B}$, and a third differential pair, C and $\overline{C}$, wherein A starts in the first track, B starts in the second track, $\overline{A}$ starts in the third track, C starts in the fourth track, $\overline{B}$ starts in the fifth track and $\overline{C}$ starts in the sixth track. A first twisting structure causes A and $\overline{A}$ to interchange, so that $\overline{A}$ is in the first track, B is in the second track, A is in the third track, C is in the fourth track, $\overline{B}$ is in the fifth track and $\overline{C}$ is in the sixth track.

[0019] In a variation on this embodiment, the first twisting structure is located approximately one half of the way down the set of parallel tracks.

[0020] In a variation on this embodiment, the first twisting structure is located more than one half of the way down the set of parallel tracks.

[0021] In a variation on this embodiment, the set of parallel tracks are located within the same metal layer in the semiconductor chip, and the one or more twisting structures use at least one other metal layer to interchange signals between tracks.

BRIEF DESCRIPTION OF THE FIGURES

[0022] FIG. 1 illustrates an untwisted wire set.

[0023] FIG. 2 illustrates a fully-twisted wire set.

[0024] FIG. 3 illustrates an intertwisted wire set in accordance with an embodiment of the present invention.

[0025] FIG. 4 illustrates a pairwise-minimal intertwisted wire set in accordance with an embodiment of the present invention.

[0026] FIG. 5 illustrates a three-way-minimal intertwisted wire set in accordance with an embodiment of the present invention.

[0027] FIG. 6 illustrates a wire twist in accordance with an embodiment of the present invention.

[0028] FIG. 7 illustrates an untwisted wire set in accordance with an embodiment of the present invention.

[0029] FIG. 8A illustrates a bend in a set of parallel tracks.

[0030] FIG. 8B illustrates another bend in a set of parallel tracks.

[0031] FIG. 8C illustrates a bend in a set of parallel tracks in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0032] The following description is presented to enable any person skilled in the art to make and use the invention, and is provided in the context of a particular application and its requirements. Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the present invention. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

Intertwisted Wire Set

[0033] Although the conventional fully-twisted wire set illustrated in FIG. 2 works reasonably well, it fully exposes each wire to its complement. As a

result, on any wire's transition, the capacitance between that wire and its neighboring complement will *always* be maximal.

[0034] More specifically, assuming a line-to-grounded-line coupling capacitance of C_c for the full length of the wire, and assuming all wires are homogenous so that C_c is the same for each pair of wires, in the fully-twisted scheme any switching wire will have a total effective coupling capacitance of $3C_c$. Of this coupling capacitance, $2C_c$ is due to its complement, because its complement moves in the opposite direction, and C_c is due to its neighbor because exactly half of its neighbor will switch in the opposite direction (causing an effective capacitance of $2C_c$ for half the length of the wire) and the other half switches in the same direction (causing an effective capacitance of zero), or its neighbor does not switch, in which case the entire length of the wire still has an effective capacitance of C_c to its unrelated neighbor.

[0035] By contrast, the intertwisted wire set illustrated in FIG. 3 interleaves wires pairwise to break apart this close coupling between a wire and its complement. As with the fully-twisted scheme illustrated in FIG. 2, a voltage step on either wire set A or wire set B will introduce no net coupling on the other wire set.

[0036] In addition, a significant improvement arises from the interleaving of two pairs of wires. This interleaving separates A from its complement $\overline{A}$, as well as B from its complement $\overline{B}$. Hence, when A moves up and $\overline{A}$ moves down, they do not suffer from the increased capacitance cost present in the fully-twisted scheme. This means that the intertwisted scheme consumes less power to charge this capacitance, and furthermore takes less time to transmit voltage signals down the wire. Consequently, in the intertwisted scheme, any wire's coupling capacitance is $2C_c$, which is about a 30% improvement. This is the same as if both neighboring wires were grounded.

[0037] Note that this intertwisted scheme saves quite a bit of energy and delay, since coupling capacitance makes up close to 70% of the total wire capacitance in modern technologies with tall wires. Moreover, this intertwisted scheme rejects noise just as well as the fully-twisted scheme does.

Pairwise-minimal Intertwisted Wire Set

[0038] For wire systems that care about differential noise but not common-mode noise, a simpler pattern can reduce the number of twists with no loss in differential noise rejection. FIG. 4 illustrates this "pairwise-minimal intertwisted" scheme in accordance with an embodiment of the present invention. In this scheme, only wire set A is twisted, while wire set B runs straight through. As with the intertwisted scheme, wire sets A and B do not interfere differentially with each other and they also do not couple into themselves, which reduces capacitance and thereby saves power and delay.

[0039] In this scheme, there are fewer twists, and hence fewer wire obstructions on the metallization layers immediately above and below the wires A and B. On the other hand, the drawback is that if wire B switches up (and $\overline{B}$ switches down), then wires A and $\overline{A}$ see a uniform upward disturbance. Note that this is not a differential noise, but a common-mode noise, which can often be ignored in digital systems.

[0040] In the FIG. 4, wire C represents the bottom of the next pair of wire sets. Note that this pattern can be repeated with no differential coupling between repeated patterns.

Three-way-minimal Intertwisted Wire Set

[0041] FIG. 5 illustrates a "three-way-minimal intertwisted"' wire set in accordance with an embodiment of the present invention. This three-way-

minimal intertwisted wire set offers the same benefits in rejecting differential noise as the pair-wise-minimal intertwisted scheme illustrated in FIG. 4. Except here, wire sets *A*, *B*, and *C* can coexist with no differential coupling between each other, while only paying the cost of a single twist among them. Like the pairwise-minimal intertwisted scheme, this three-way-minimal intertwisted scheme does not reject common-mode noise.

[0042] In FIG. 5, wire *D* represents the bottom of the next three-way pattern of wire sets. Note that this pattern can be repeated with no differential coupling between repeated patterns.

[0043] Also note that the wires need not be part of the same bus that transmits from location *X* to location *Y* on a chip. In particular, if wires *A* and $\overline{A}$ are part of a bus from *X* to *Y*, and wires *B* and $\overline{B}$ are part of a different bus, either running in the reverse direction (from *Y* to *X*), or even to and from wholly different sources and receivers, the scheme is still applicable. To minimize noise as well as delay and power, the wires need only twist in an interleaved fashion.

Wire Twists

[0044] As is illustrated in FIG. 6, in one embodiment of the present invention a wire twist requires side routes in another routing layer to accomplish a twist between wires *A* and $\overline{A}$ across an intervening wire *B*. More specifically, the wire *A* moves from the first track to the third track directly, without a side route through another layer. The wire *B* does not changes tracks, but passes under (or over) the wire *A*. This is accomplished by passing through a via (indicated by cross-hatching) to another routing layer (indicated by a diagonal pattern) before returning through another via to its original layer. The wire $\overline{A}$ similarly passes (from left to right) through a via into a vertical strip in the other layer, which

passes under (or over) wire *B* and then passes underneath wire *A* for some distance before returning through a via to its original layer.

[0045] Note that in technologies that allow wires at 45 degrees, twists can cost less than in this Manhattan layout. Also note that fully-landed and fully-enclosed vias typically require more room than a wire's minimum-allowed width, but these are long wires and are typically wider than minimum.

[0046] Using too few vias to connect two wires leads to poor performance. Technologies with aluminum wires use poorly-conducting tungsten vias, and consequently have resistance values of 5-10 Ohms per via. In this case, one via is certainly not sufficient, and even four may not be, either. Processes with copper help significantly, because they pour the vias in the same step as pouring the wires, making a via equivalent to an extra square of length. However, even in copper technologies it is advantageous to array many vias together, because vias serve as nucleation sites for voids that migrate down the wire during operation.

[0047] Hence, the true cost of twists is probably closer to five or more wire pitches. In a wire several thousand microns long, this may be seem insignificant but still leads to inconvenient layout constraints.

[0048] Twists also lead to a slight imbalance in the wire characteristics. With enough vias to minimize twist resistance, the effects of the twist are trivial relative to the rest of the long wire. In addition, on-chip wires are not "transmission-line-like" enough to make twists meaningful from an impedance-matching perspective.

Location of Wire Twists

[0049] For the schemes depicted in FIGs. 4 and 5, one might wonder if twisting at the mid-way point is best. Any wires that run bi-directionally would best be served by twists at the midway position.

[0050] Consider, however, in FIG. 4 the noise coupled onto $\overline{B}$ from A and $\overline{A}$, with the twist at the mid-way position. Here, we are concerned about the noise at the receiver end, or the far right, of wire $\overline{B}$. The current injected onto $\overline{B}$ from A is *closer* to $\overline{B}$'s right end than the current injected onto $\overline{B}$ from $\overline{A}$. This matters because the current injected onto $\overline{B}$ will split: some will go left, and some will go right. The farther from the right that the current enters, the less that will actually go to the right.

[0051] Note that moving the twist to the right can help because it makes more of the injected current from $\overline{A}$ go to the right to balance out the injected current from A. However, moving it too far makes the injected current from $\overline{A}$ too strong.

Twists Can Occur at Bends in Parallel Tracks

[0052] Note that a set of parallel tracks can bend (for example, by ninety-degrees) in order to connect two components on the semiconductor die. This is typically performed as is illustrated in FIGs. 8A and 8B. Note that in an integrated circuit layout it is common to have one metal layer dedicated to horizontal signal lines and another adjacent metal layer dedicated to vertical signal lines. Hence, if a wire bends by ninety degrees (from horizontal to vertical or from vertical to horizontal) a via is typically used to connect the horizontal signal line to the vertical signal line. Hence, in the examples illustrated in FIGs. 8A and 8B, note that when the set of parallel tracks bends ninety degrees, the wires move through vias (indicated by cross-hatching) to another metal layer (indicated by a diagonal pattern). Also note that the bend illustrated in FIG. 8A reverses the order of the wires, whereas the bend illustrated in FIG. 8B does not.

[0053] In the embodiment of the present invention, a true wire can be

easily exchanged with its complement by staggering the bends in the true and complement wires relative to each other so that the true and complement wires cross as is illustrated in FIG. 8C. In FIG. 8C note that signals A and $\overline{A}$ are interchanged at the ninety-degree bend. Furthermore, note that since vias are already used to perform a ninety-degree bend (as is illustrated in FIGs. 8A and 8B) no additional vias are required to accomplish this interchange, and hence there is no additional cost for this crossover.

Untwisted Wire Set

[0054] FIG. 7 illustrates an untwisted wire set in accordance with an embodiment of the present invention. In this wire set, each wire is separated from its complement by an intervening wire. For example, wire A is separated from wire $\overline{A}$ by the intervening wire B. Note that this untwisted pattern repeats for additional wires. Moreover, this untwisted pattern provides similar power reduction benefits of the previous embodiments (illustrated in FIGs. 3-6), as well as some noise cancellation benefits, without the need for twisting structures to interchange the wires.

[0055] The foregoing descriptions of embodiments of the present invention have been presented for purposes of illustration and description only. They are not intended to be exhaustive or to limit the present invention to the forms disclosed. Accordingly, many modifications and variations will be apparent to practitioners skilled in the art. Additionally, the above disclosure is not intended to limit the present invention. The scope of the present invention is defined by the appended claims.